

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A delay-locked loop circuit ~~(200)~~, comprising input means ~~(210)~~ for a signal that is to be delayed, said input means comprising means for splitting said input signal into a first and a second branch, where the signal in the first branch is connected to a component ~~(220)~~ for delaying the signal and the signal in the second branch is used as a non-delayed reference for the delay caused by the delay component in the first branch, characterized in that the delay component ~~(220)~~ is a passive tunable delay line, with the circuit comprising tuning means ~~(230)~~ for the tunable delay line, said tuning means being affected by said reference signal, and with the first branch comprising output means for outputting a delayed signal with a chosen phase delay.
2. (Currently Amended) The circuit of claim 1, in which the delay component ~~(220)~~ is continuously tunable.
3. (Currently Amended) The circuit of claim 1 ~~or 2~~, in which the delay component ~~(220)~~ is a passive component.
4. (Currently Amended) The circuit of claim 1, ~~2 or 3~~, in which the delay component ~~(220)~~ is a tunable ferroelectric delay line.

5. (Currently Amended) The circuit of ~~any of claims~~ claim 1 ~~[[4]]~~, in which the second branch comprises a phase detector ~~(250)~~, by means of which the non-delayed signal of the second branch is compared to the delayed signal in the first branch at a point in the first branch where the delay to be caused by the delay component is known, the output signal from the phase detector ~~(250)~~ being used as a control signal for the tuning means for the delay component of the first branch.